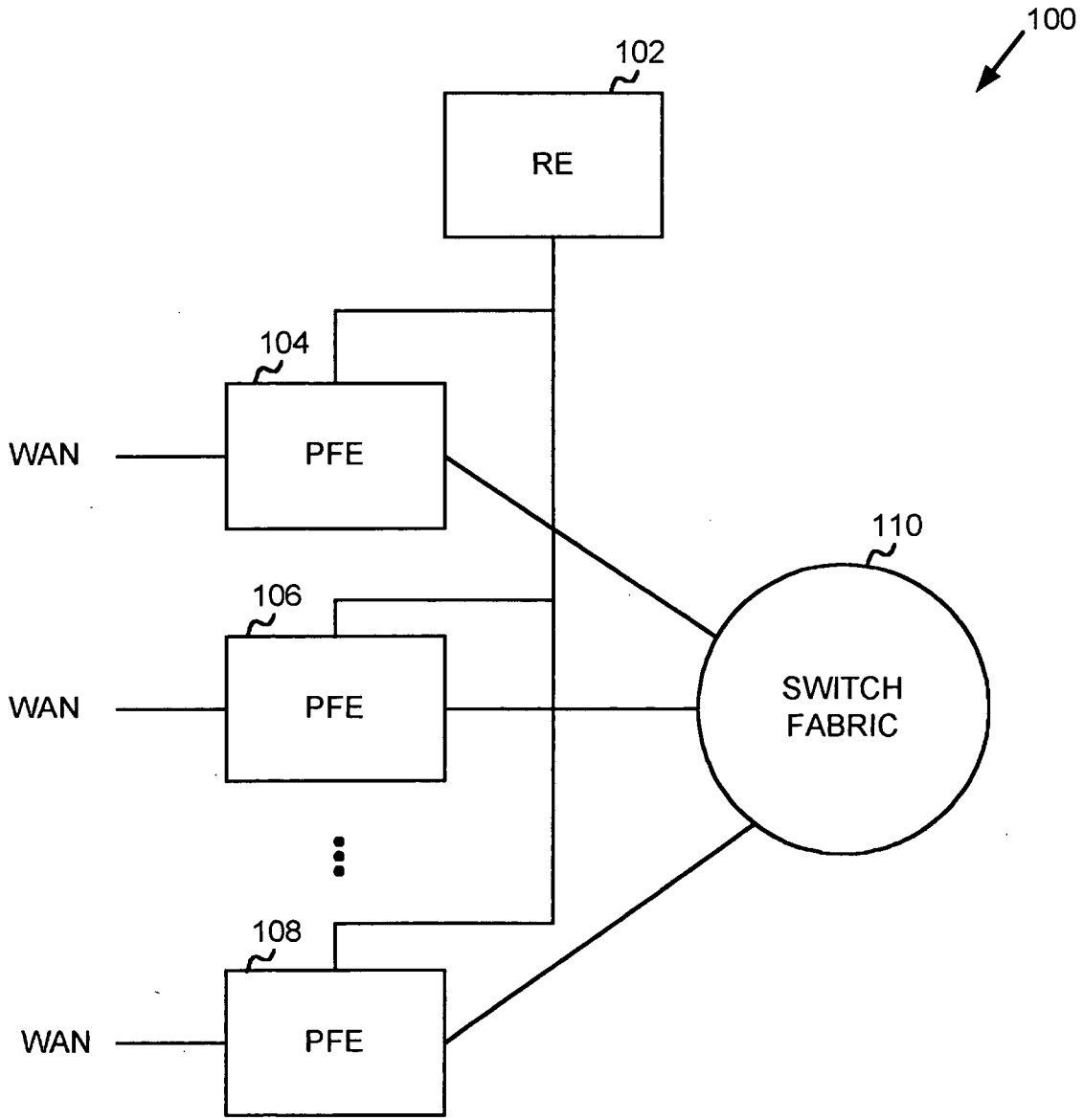

100
102
RE
104
WAN
PFE
106
WAN
PFE
110
SWITCH
FABRIC
108
WAN
PFE

Fig. 1

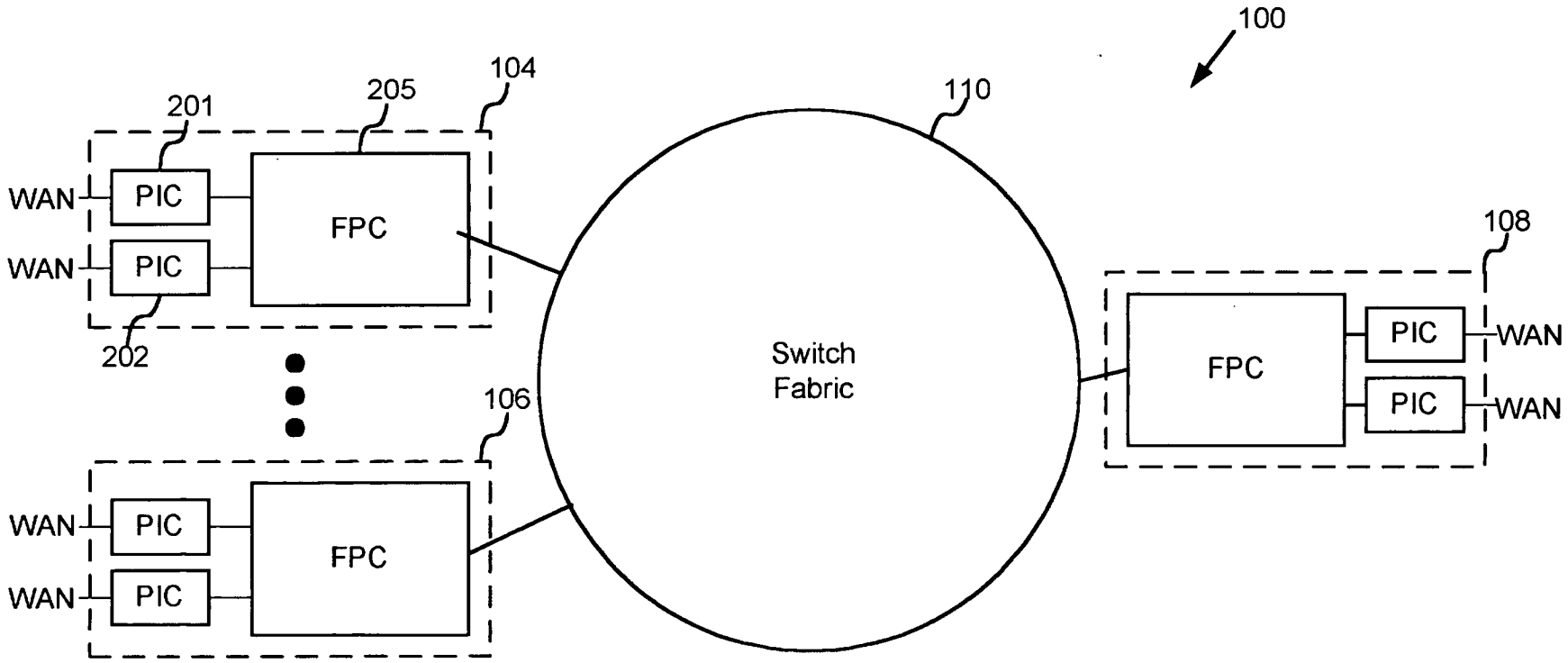
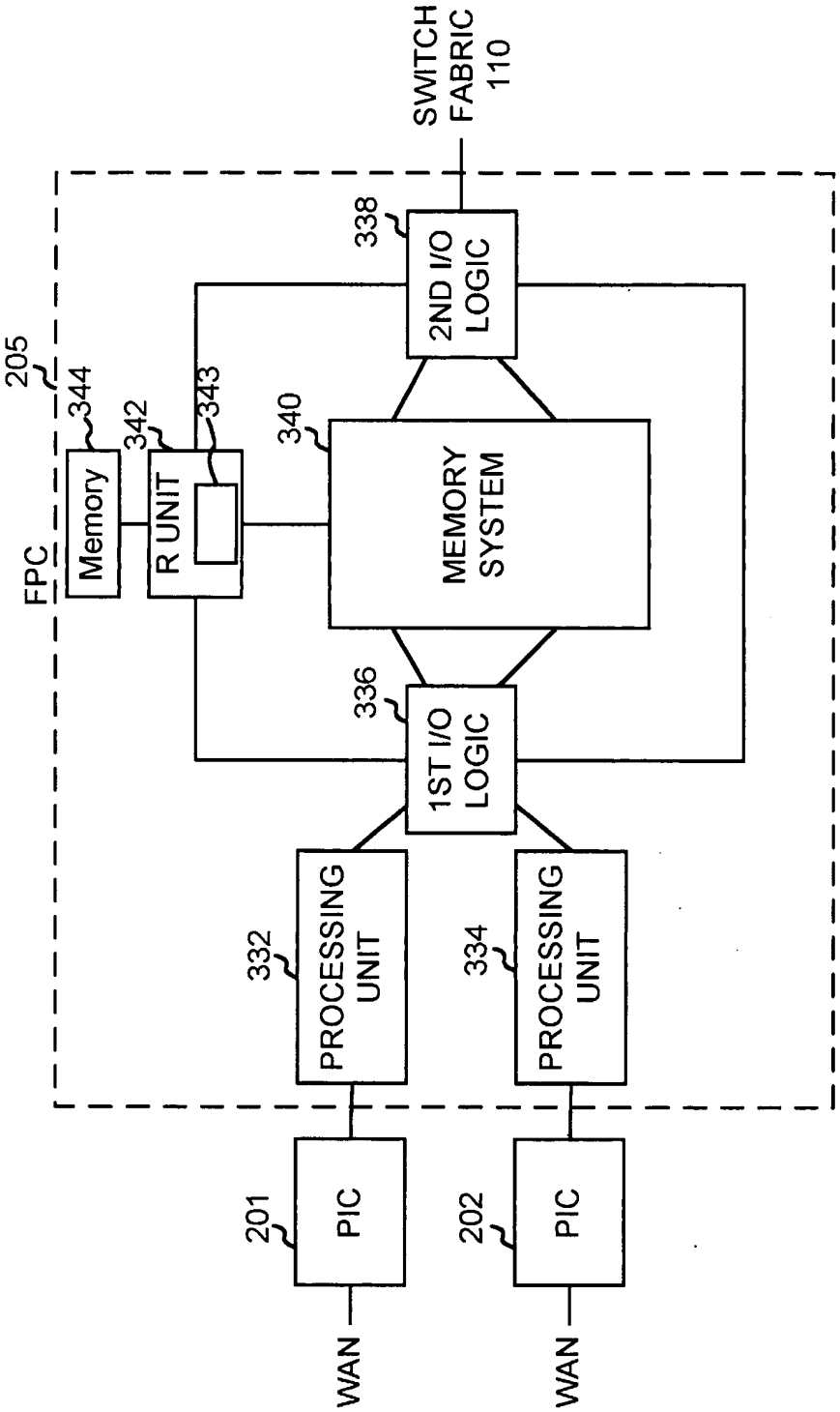

100
104
201
205
110
WAN
PIC
FPC
WAN
PIC
202
108
Switch
Fabric
PIC
WAN
FPC
PIC
WAN
106
WAN
PIC
FPC
WAN
PIC

Fig. 2

Fig. 3


SWITCH FABRIC 110
205
FPC
Memory
344
R UNIT
342
343
340
MEMORY SYSTEM
338
2ND I/O LOGIC
336
1ST I/O LOGIC
332
PROCESSING UNIT
334
PROCESSING UNIT
201
PIC
202
PIC
WAN
WAN

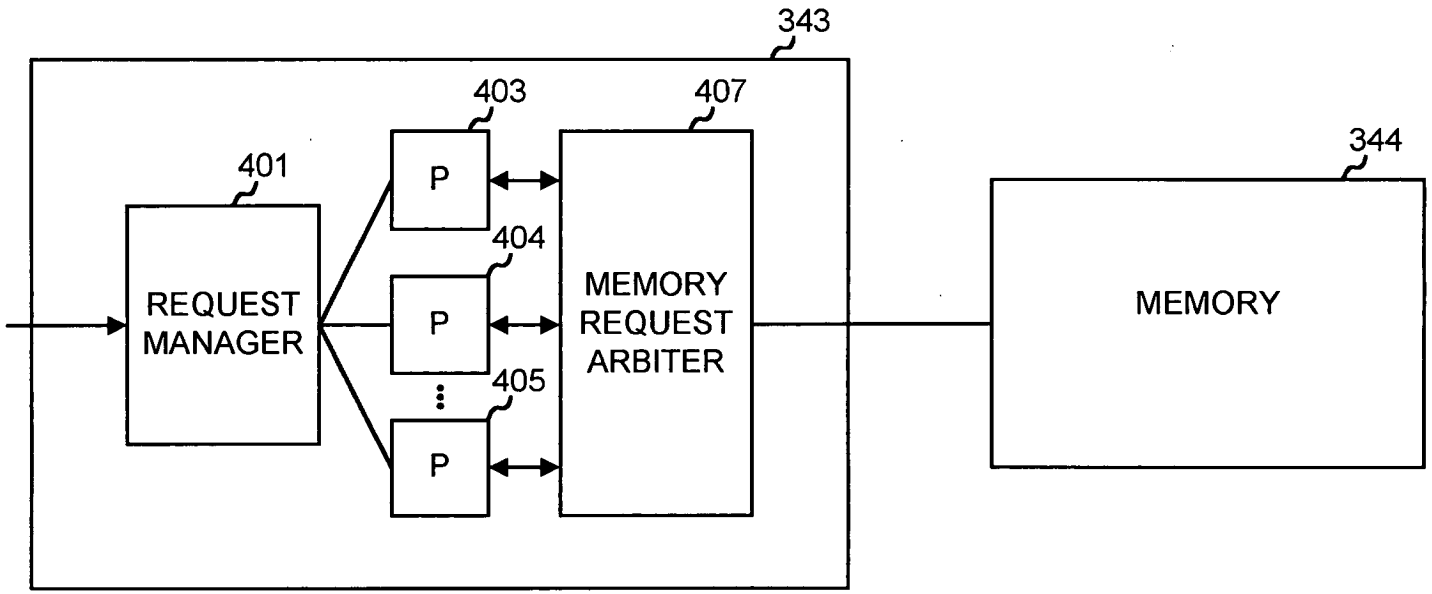

343
403
407
401
344
P
404
REQUEST
MANAGER
P
MEMORY
REQUEST
ARBITER
MEMORY
405
P

Fig. 4

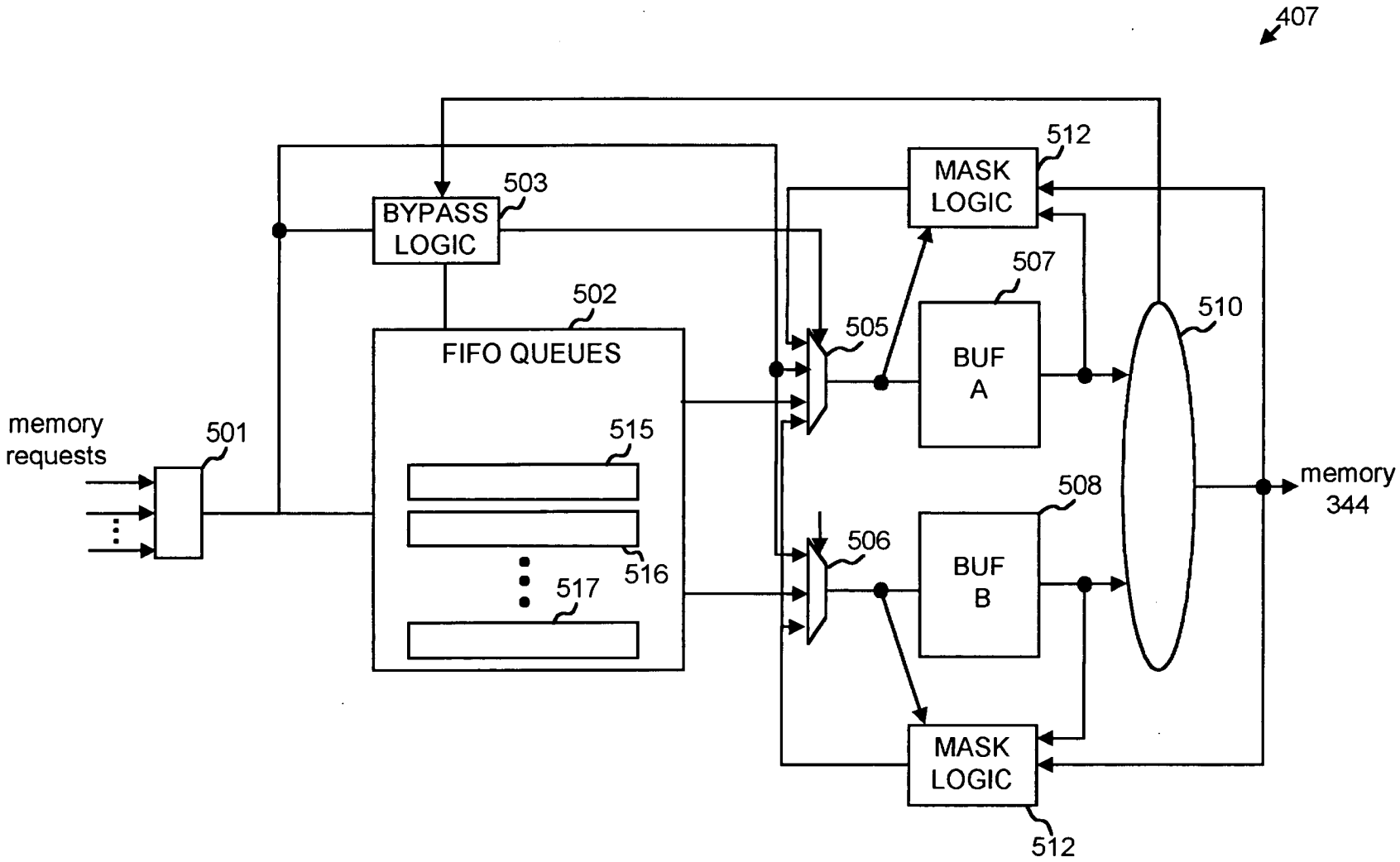

407
512
MASK LOGIC
503
BYPASS LOGIC
507
502
505
510
FIFO QUEUES
BUF A
memory requests
501
515
memory 344
508
506
516
BUF B
517
MASK LOGIC
512

Fig. 5

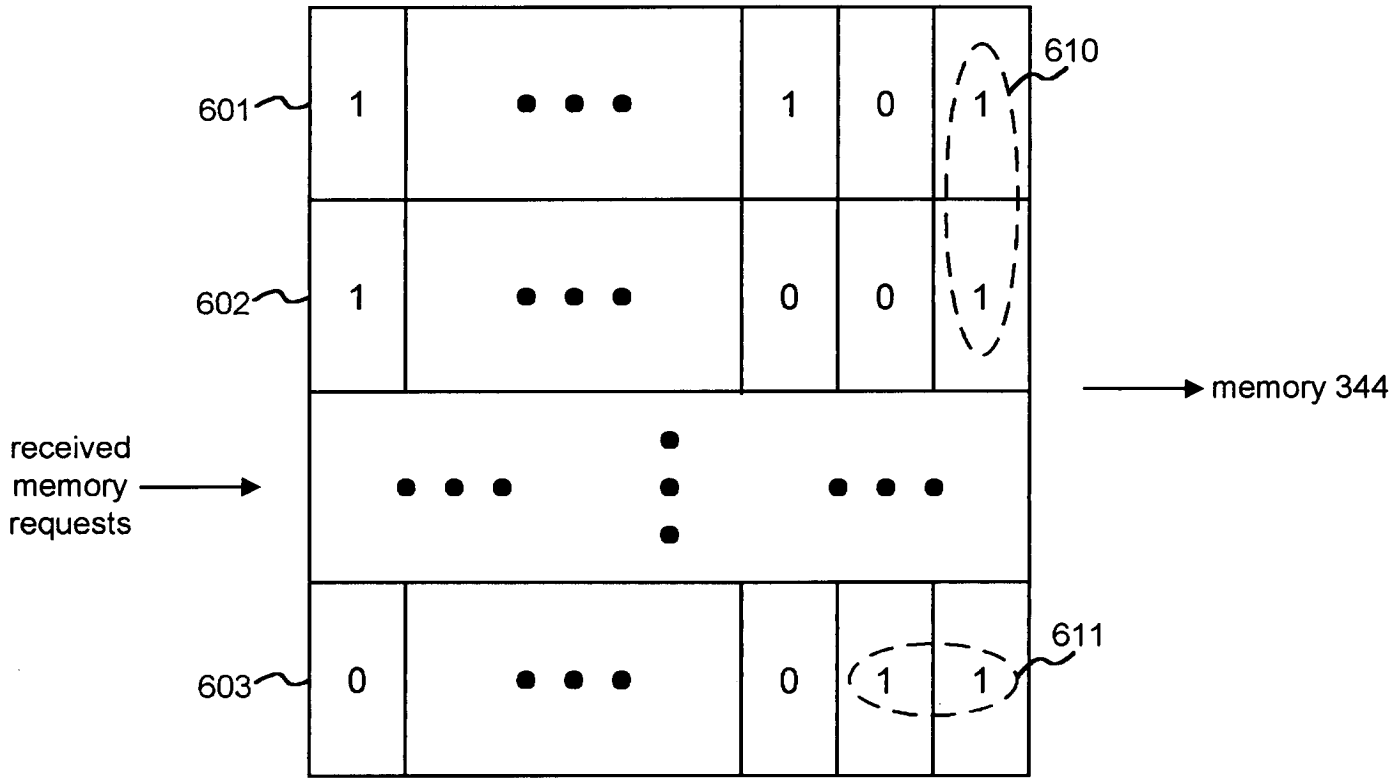

601
602
603
1
1
0
1
0
1
1
0
0
1
0
0
1
1
610
611
received
memory
requests
memory 344

Fig. 6

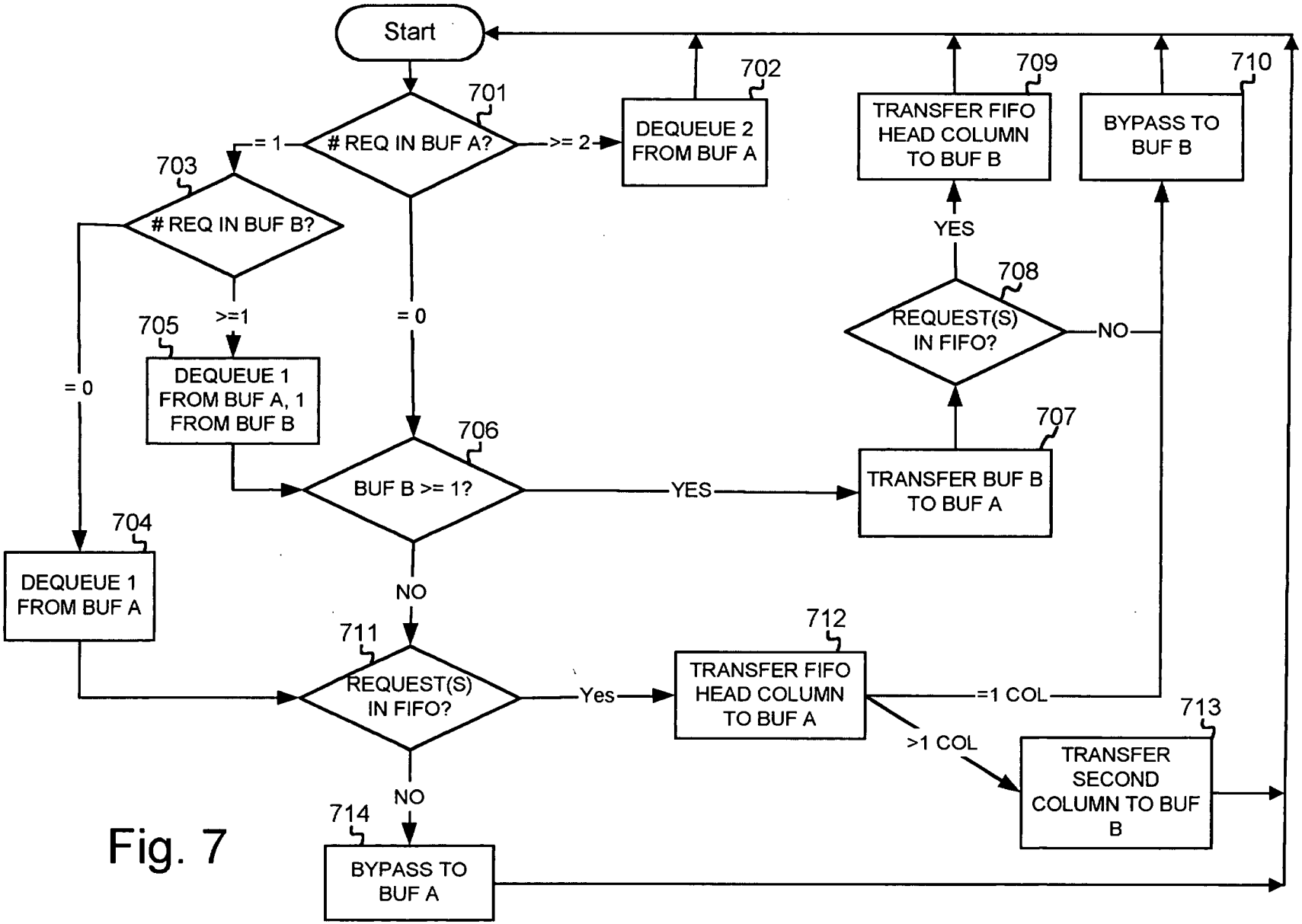


Fig. 7

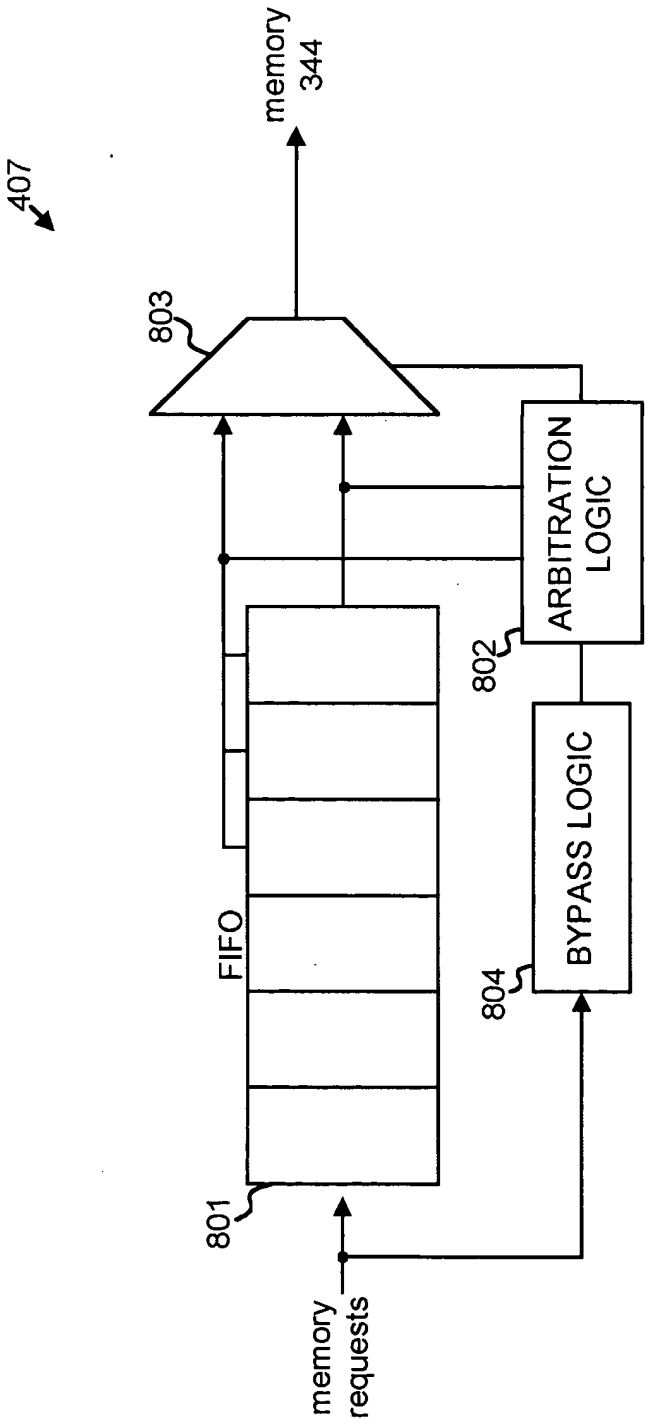

407
memory
344
803
ARBITRATION
LOGIC
802
BYPASS LOGIC
804
FIFO
801
memory
requests

Fig. 8